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WHAT IS CLAIMED IS:

1 A method of transferring bursts of data between a 2

- processor device and a FIFO device, said transfer comprising:
- triggering a burst transfer from the change of state of a 3
- FIFO output signal, said change of state being the occurrence 4
- of a triggering event within the FIFO device; and 5
- 6 inhibiting of triggering of any further burst transfers
- until a current burst transfer is complete.
- 1 The method of claim 1, wherein:
- 2 said triggering event is change in a FIFO fullness
- 3 indicator flag.
- 1 3. The method of claim 2, wherein:
- said FIFO fullness indicator flag denotes the FIFO is 2
- less than or greater than half full; and 3
- said triggering event is changing from said FIFO fullness 4
- indicator flag denoting less than half full to greater than 5
- 6 half full.
- 1 The method of claim 2, wherein:
- 2 said fullness indicator denotes less than or greater than
- half full; and 3
- 4 said triggering event is changing from said FIFO fullness
- indicator flag denoting greater than half full to less than 5
- 6 half full.

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- 1 5. The method of claim 1, wherein:
- 2 said burst transfer includes transfer of predetermined
- 3 amount of data in fixed number of sequential clock cycles.
- 1 6. The method of claim 5, wherein:
- 2 said predetermined amount of data in a burst transfer is
- 3 set by an input to the FIFO device from the processor device
- 4 during initialization.
- 1 7. The method of claim 5, wherein:
- 2 said predetermined amount of data in a burst transfer is
- 3 set by an input to a programmable FIFO device register.
- 1 8. The method of claim 7, wherein:
- 2 the processor device supplies aid predetermined amount of
- 3 data to said programmable FIFO device register via an output
- 4 pin.
- 9. The method of claim 1, further comprising the step
- 2 of:
- 3 inhibiting trigger from processor device, thereby
- 4 inhibiting further burst transfers until a predetermined
- 5 number of clock cycles following completion of current burst
- 6 transfer.